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⑤4発明の名称　半導体素子の製造方法

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明細書

1．発明の名称

半導体素子の製造方法

2．特許請求の範囲

(1) シリコンウェハの表面に熱酸化膜を形成する工程を含む半導体素子の製造方法において、前記熱酸化膜を形成する工程の直前に、水素を含む雰囲気中で前記シリコンウェハを1100［℃］以上の温度で熱処理することを特徴とする半導体素子の製造方法。

(2) 前記熱処理の時間を、1分以下に設定したことを特徴とする特許請求の範囲第1項記載の半導体素子の製造方法。

(3) 前記熱酸化膜は、ゲート酸化膜であることを特徴とする特許請求の範囲第1項記載の半導体素子の製造方法。

(4) 前記熱処理するに際し、ハロゲンランプ等の光加熱により前記シリコンウェハの表面を1100［℃］以上の温度に加熱することを特徴とする特許請求の範囲第1項記載の半導体素子の製造方法。

3．発明の詳細な説明

〔発明の技術分野〕

本発明は、半導体素子の製造方法に係わり、特にシリコンウェハの表面に形成される熱酸化膜中の欠陥発生を抑えた半導体素子の製造方法に関する。

〔発明の技術的背景とその問題点〕

従来、ゲート酸化膜を形成する場合、ゲート酸化の直前にRCA処理（文献：N．Kern and D．W．Puotinen，"RCA Review"，31，187（1970））等の薬品による清浄を行った後、純水洗浄を行っている。この場合、純水洗浄によって、必ず自然酸化膜が7～15［Å］形成されることになる。

一方、近年の半導体集積回路の高集積化は目覚ましく、素子の微細化及び薄膜化に対する要求は極めて厳しいものがある。そして、高集積回路に用いられるゲート酸化膜の厚さとして100［Å］以下を要求される場合もでている。このため、前

記した自然酸化膜のゲート酸化膜に及ぼす影響は大きい。

また、前記純水洗浄を省略し、弗酸系薬品によって自然酸化膜を除去した後に直後ゲート酸化に至る場合、シリコンウェハの表面は不飽和結合を多く有し、極めて活性な表面となっている。その結果、シリコンウェハの表面は汚染物質が被着し易くなっている。従って、このような表面上に形成されたゲート酸化膜は、初期短絡不良を示す欠陥が多くなってしまう。

（発明の目的）

本発明は上記の事情を考慮してなされたもので、その目的とするところは、熱酸化膜の形成工程でその酸化膜に取り込まれる欠陥を効果的に低減することができ、素子特性の向上等をはかり得る半導体素子の製造方法を提供することにある。

（発明の概要）

本発明の骨子は、シリコンウェハを水素雰囲気中で熱処理することにより、シリコンウェハ表面の不飽和結合に水素を結合させ、熱酸化膜を形成

する際の電気伝導上の欠陥発生を抑制することにある。

即ち本発明は、シリコンウェハの表面に熱酸化膜を形成する工程を含む半導体素子の製造方法において、前記熱酸化膜を形成する工程の直前に、水素を含む雰囲気中で前記シリコンウェハを１１００［℃］以上の温度で（望ましくは１分以下の時間）熱処理するようにした方法である。

（発明の効果）

本発明によれば、より確実に理想に近い状態でシリコンウェハの表面を自然酸化膜がなく且つ不活性な状態に制御することができるので、該ウェハ上に形成する熱酸化膜の欠陥発生を低減することができ、特に１００［Å］以下の薄い熱酸化膜を十分な耐圧を持たせて作ることができる。このため、ＭＯＳ集積回路等の信頼性向上、微細化及び高集積化をはかることができる。

（発明の実施例）

以下、本発明の詳細を図示の実施例によって説明する。

第１図（ａ）～（ｅ）は本発明の一実施例方法に係わるＭＯＳキャパシタ製造工程を示す断面図である。まず、ＣＺ法により形成されウェハ状に切り出された面方位（１００），比抵抗５～２０［Ω㎝］のシリコンウェハを用い、１０００［℃］で水素燃焼酸化を１００分間行い、第１図（ａ）に示す如くシリコンウェハ１１の表面に厚さ５０００［Å］の熱酸化膜１２を形成した。

次いで、第１図（ｂ）に示す如く全面にレジスト１３を塗布したのち、写真蝕刻法によりゲート酸化膜形成領域の酸化膜１２をエッチング除去した。その後、第１図（ｃ）に示す如くＲＣＡリンス処理と水洗により上記シリコンウェハ１１を洗浄した。このとき、ウェハ１１の露出表面には、薄い自然酸化膜１４が形成される。

次いで、シリコンウェハ１１の表面に、例えばハロゲンランプを照射し、ウェハ表面温度を１１００［℃］まで上昇させ、1.0［％］の水素を含むアルゴンガス中に１分間晒し、第１図（ｄ）に示す如く前記自然酸化膜１４を除去した。この

とき、シリコンウェハ１１の表面の不飽和結合には水素原子が結合されることになる。

次いで、上記第１図（ｄ）に示す工程の直後に、２０［％］の乾燥酸素を含むアルゴンガス中で９００［℃］２０分間シリコンウェハ１１を酸化し、第１図（ｅ）に示す如くシリコンウェハ１１の表面に厚さ４０［Å］の熱酸化膜（ゲート酸化膜）１５を形成した。続いて、多結晶シリコン膜１６をＬＰＣＣＶＤ法により約０．４［μｍ］形成した。さらに、例えば１０００［℃］１０分間のＰＯＣℓ₃拡散法により、多結晶シリコン膜１６の抵抗を低下させた後、写真蝕刻法によりゲート電極パターンを形成した。

上記形成された試料の耐圧不良率を測定したところ、第２図に示す如き結果が得られた。ここで、図中Ａは本実施例による場合、Ｂは従来例の場合である。なお、いずれの場合も、ゲート面積は１０［㎟］、ゲート酸化膜厚は５０［Å］とした。第２図から判るように、本実施例の場合、従来例に比して、酸化膜の耐圧不良率が飛躍的に改

善されることが判る。

このように本実施例方法によれば、シリコンウェハ11の表面に形成される熱酸化膜15の欠陥密度を著しく低減させることができる。このため、半導体集積回路の高集積化に大きな効果が得られる。例えば、ゲート酸化膜の薄膜化を容易にし、MOS素子の動作特性向上及び信頼性の向上が可能となる。

なお、本発明は上述した実施例方法に限定されるものではない。例えば、希釈不活性ガスとして、アルゴンを用いたが、その他ネオン、ヘリウム等の貴ガスは勿論、窒素等の活性度の低いガスを用いてもよい。さらに、ゲート電極として、リン添加多結晶シリコンを用いたが、Al、Mo、W等の高融点金属若しくはそのシリサイドを用いてもよい。また、ゲート酸化膜等の熱酸化膜形成前の熱処理温度は1100[℃]に限るものではなく、それ以上の温度であればよい。さらに、このときの処理時間は、高温熱処理による半導体ウェハへの種々の影響を考慮すると1分以下の短時間とするのが望ましい。

また、実施例ではMOSキャパシタの製造に応用したが、MOSFET及びMOS集積回路は勿論のこと、他の熱酸化膜を有する半導体素子の製造に適用することが可能である。その他、本発明の要旨を逸脱しない範囲で、種々変形して実施することができる。

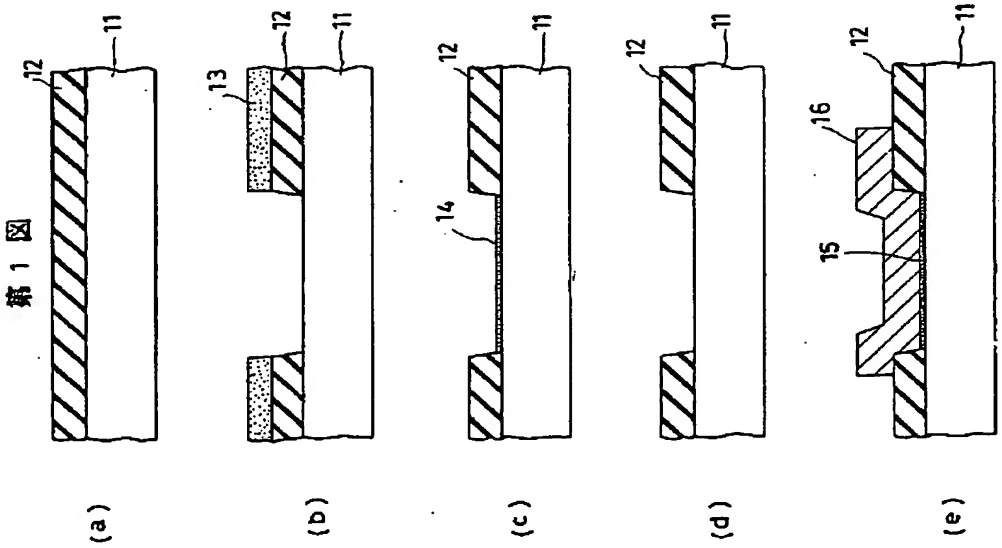
4．図面の簡単な説明

第1図（a）～（e）は本発明の一実施例方法に係わるMOSキャパシタ製造工程を示す断面図、第2図は上記実施例の効果を説明するためのもので熱酸化膜の耐圧不良率を示す特性図である。

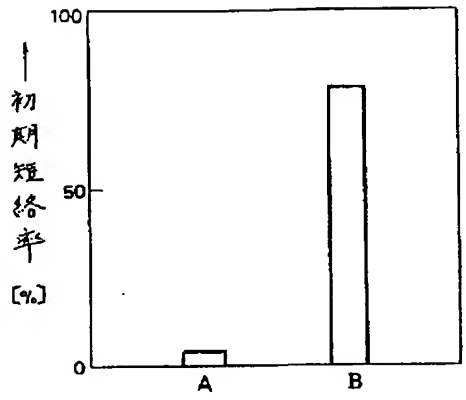
11…シリコンウェハ、12…熱酸化膜、13…レジスト、14…自然酸化膜、15…熱酸化膜（ゲート酸化膜）、16…燐加多結晶シリコン膜（ゲート電極）。

出願人代理人　弁理士　鈴江武彦

第1図



第 2 図



PATENT ABSTRACTS OF JAPAN

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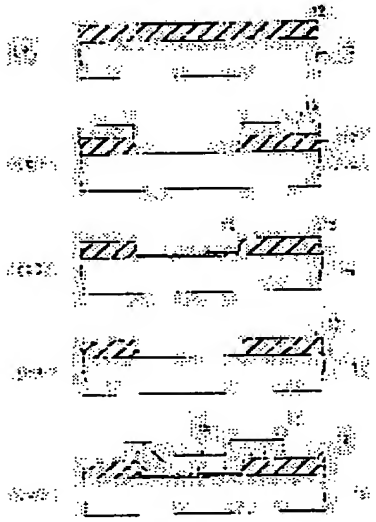
(54) MANUFACTURE OF SEMICONDUCTOR ELEMENT

(57)Abstract:
PURPOSE: To suppress the generation of lattice defects related to conductivity in a process of the formation of a thermal oxide film by a method wherein hydrogen is caused to join unsaturated bonds in a silicon wafer surface when the silicon wafer is subjected to heat treatment in a hydrogen atmosphere.
CONSTITUTION: A thermal oxide film 12 is formed on the surface of a silicon wafer 11, a resist 13 is applied to the entire surface, and then etching is accom plished for the removal of the thermal oxide film 12 from a region planned for the formation of a gate oxide film. The silicon wafer 11 is then subjected to an RCA rinse and washing with water for the formation of a thin natural oxide film 14. Next, the wafer 11 is irradiated with light from a lamp, a halogen lamp for example, for the rise of the wafer surface temperature up to 1,000[° C], and is left for a minute in argon gas including some hydrogen. In this process, unsaturated bonds present in the surface of the silicon wafer 11 accept hydrogen atoms for saturation. Next, a thermal oxide film 15 is formed on the wafer surface,which is followed by the formation of a polycrystalline silicon film 16.



LEGAL STATUS

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[Date of final disposal for application]

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[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] The annealing approach of the InP single crystal characterized by heat-treating an InP ingot or an InP wafer at 800-degree-C or more temperature of 1060 degrees C or less.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the annealing approach of removing the stress in an InP single crystal.
[0002]
[Description of the Prior Art] An InP single crystal substrate grows up an epitaxial layer mainly on it, and is used as a substrate for manufacturing semiconductor laser. However, if surface morphology is bad when growing up an epitaxial layer on the single crystal substrate with which stress exists, problems -- a good electrical property is not acquired -- arise. It is generated with the thermal stress under single crystal growth, and the stress in a single crystal substrate remains during a crystal, without being eased also after it processes it in the shape of [thin] a wafer. In order to obtain a single crystal substrate without stress, it is necessary to raise a single crystal on the conditions that thermal stress is small but, and in order to raise a single crystal under the big temperature gradient of 50 degrees C/cm or more in the case of an LEC method, it is not avoided that big thermal stress is applied and stress occurs. Productivity of the problem was very bad although there were the vapor pressure control LEC method and perpendicular Bridgman method which raise an InP single crystal under inclination whenever [low-temperature / with small thermal stress] and which perform an LEC method in the Lynn ambient atmosphere as approaches.
[0003]
[The technical problem which invention will solve and to carry out] The purpose of this invention offers the approach of manufacturing an InP single crystal substrate without stress for high productivity. It mentioned above that there were a vapor pressure control LEC method and a perpendicular Bridgman method as a single crystal growth method which stress does not produce. B-2 O3 which is liquid encapsulant when the temperature gradient of a crystal training interface is made small in an LEC method Upside temperature becomes high and it is B-2 O3. Lynn will slip out from the front face of a single crystal ingot out of which it came upwards. In order to prevent this Lynn omission, the vapor pressure control LEC method applied the moderate partial pressure of the Lynn steam into the ambient atmosphere. In order to prevent the steam of Lynn pulling up in this approach, and condensing to a furnace wall, the interior is made into double structure, and the device maintained at the temperature to which Lynn does not condense an inside wall is required, and it is necessary to devise a seal to the appearance to which the Lynn steam does not leak from an inside wall further. Thus, as a result of the structure in a furnace becoming complicated, cleaning in the furnace for every single crystal growth becomes complicated, and the problem that the operating ratio of a furnace falls arises. Moreover, as a result of making small the temperature gradient at the time of single crystal growth, the diameter controllability worsened, therefore the probability of polycrystal-izing or twin crystal generating became high, and the problem that single crystal yield falls is also produced.
[0004] Polycrystal generates a perpendicular Bridgman method from the part by the wetting of a raw material and a crucible, and single crystal yield has come [on the other hand] to be put in practical use as means of production of a single crystal very low. An LEC method is the only thing which is the technique in which productivity is the highest, and is used for raising an InP single crystal although current and an InP single crystal are produced. However, since the temperature gradient of a crystal growth interface is large in cm and 50 degrees C /or more, stress will occur with thermal stress. As mentioned above, by the single-crystal-growth approach that single crystal yield is high, stress arises during a crystal and there is a problem that single crystal yield is very bad, in a single crystal growth method which stress does not generate. This invention is an approach for obtaining the single crystal substrate which solves the above-mentioned problem and does not have stress by high yield.

[0005]
[Means for Solving the Problem] MLEC which impressed the usual big LEC method or usual big magnetic field of a temperature gradient where single crystal growth was excellent in productivity in this invention -- it supposes that it carries out by law and the stress produced during single crystal growth by subsequent annealing is removed. Although ingot annealing had already been performed in GaAs, this purpose improves the homogeneity of an electrical property chiefly, and it was not performed in order to remove stress (refer to JP,51-142270,A, JP,61-8917,A, and JP,61-185923,A).
[0006] As a result of repeating various examination, the artificer found out that the stress produced during single crystal growth was removable by annealing at the temperature below 800-degree-C or more melting point. ****** [annealing / the ingot which raised the single crystal is still sufficient as it, and] after processing this annealing in the shape of a wafer. On the occasion of annealing, it is necessary to prevent that Lynn evaporates from a crystal front face in annealing. As the means, annealing is performed in the Lynn steam of the pressure more than the dissociation pressure of InP, or a phosphine ambient atmosphere, or it is B-2 O3. The method of performing annealing in inside is raised. Furthermore, a programming rate and a cooling rate should avoid rapid heating quenching, and should select it within limits in which a crystal does not receive stress. Although specifically based also on the magnitude of a crystal, the programming rate should be carried out in 100 degrees C /or less, and the cooling rate should be carried out in 50 degrees C/o'clock or less o'clock. Moreover, as for the case of a wafer, in the case of an ingot, for 20 - 60 minutes is usually required for 15 to 30 hours that, as for annealing time amount, a crystal should just become homogeneity temperature.
[0007]
[Function] By carrying out temperature management strictly, this invention prevents distorted generating under crystal by maintaining a crystal to equilibrium.
[0008]
[Example] The S dope InP single crystal ingot raised in the example 1 LEC method was heat-sealed with the degree of vacuum of 1x10-5Torr in quartz ampul with red phosphorus. When it all evaporated in annealing temperature, the red phosphorus put in at this time adjusted the amount so that it might become one atmospheric pressure. The ampul heat-sealed succeedingly was set in the soaking pit, and 1000 degrees C and annealing of 20 hours were performed. The programming rate at this time carried out [degrees C / // 100] the cooling rate in 50 degrees C/o'clock in o'clock. After [annealing termination] periphery grinding and a slice were performed, and, finally the double-sided mirror wafer with a thickness of 350 micrometers was made. On the other hand, after raising in an LEC method, the ingot which did not perform annealing was processed similarly and the double-sided mirror wafer with a thickness of 350 micrometers was made to it. Although slip line-like stress was seen by the wafer which did not perform annealing at the periphery as a result of observing both stress with an infrared transmission method, stress was not observed at all by the wafer which performed annealing.
[0009] Only the Sn dope InP single crystal ingot raised in the example 2 LEC method was heat-sealed in quartz ampul with the degree of vacuum of 1x10-5Torr. The ampul heat-sealed succeedingly was set in the soaking pit, and 800 degrees C and annealing of 20 hours were performed. The programming rates and cooling rates at this time are 100 degrees C/[o'clock and] and 50 degrees C/o'clock, respectively. The double-sided mirror wafer with a thickness of 350 micrometers was made to this ingot after annealing termination. Moreover, the ingot which did not perform annealing also observed finishing and stress to the double-sided mirror wafer with a thickness of 350 micrometers. Consequently, although the stress of the symmetry was observed 4 times by the wafer which did not perform annealing, stress was not observed with the wafer which performed annealing.
[0010] When the Sn dope InP single crystal ingot raised in the example 3 LEC method was processed into the double-sided mirror wafer with a thickness of 350 micrometers and stress was observed, the stress of the symmetry was observed 4 times. It is PH3 about this wafer. 900 degrees C and annealing for 30 minutes were performed in the air current. The programming rates and cooling rates at this time are 50 degrees C/ [o'clock and] and 30 degrees C/o'clock, respectively. It did not try to be removed by stress when the stress of this wafer was again observed after annealing termination.
[0011]
[Effect of the Invention] By the annealing approach of this invention, the stress produced during single crystal growth can be removed, and an InP single crystal substrate without stress can be manufactured by high yield. By using this single crystal substrate, upgrading and the improvement in yield in an epitaxial layer are attained, and the improvement in the engine performance and the improvement in yield of a device

in a laser diode etc. are attained.

[Translation done.]